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Application of

Applicant : Joseph M. Brand
Serial No. : 09/335,618
Filed : June 18, 1999
Title : ENCAPSULANT LOCK FEATURE
Docket No. : MIO 0051 PA
Examiner : Alonzo Chambliss
Art Unit : 2814

Assistant Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF FACSIMILE
I hereby certify that this correspondence is being facsimiled to (703) 308-7722, on May 17, 2001.

Attorney 42,695 Reg. No.

Sir:

AMENDMENT

This paper is being filed in response to the Office Action of March 9, 2001. Reconsideration of the present application is respectfully requested in light of the amendments and remarks below.

In the specification

Please replace the title of the invention with ---SEMICONDUCTOR DEVICE UTILIZING AN ENCAPSULANT FOR LOCKING A SEMICONDUCTOR DIE TO CIRCUIT SUBSTRATE---.

In the Claims

The entire set of presently pending claims has been reproduced below for the convenience of the Examiner. Amended claims, new claims, and canceled claims are indicated as such in the parenthetical following each claim number. Attached hereto as appendix A is a marked-up reproduction of the claims illustrating changes made to the claims.

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1. (Amended) A packaged semiconductor device comprising:
a semiconductor chip;
a laminate defining first and second major faces, said laminate including
an electrically conductive layer,
an underlying substrate supporting said electrically conductive layer, and
at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate and through said second major face; and
an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend through said void from said first major face to said second major face and contacting said underlying substrate.

4. A packaged semiconductor device as claimed in claim 1 wherein said contact between said encapsulant and said underlying substrate is characterized by an adhesive bond.

5. A packaged semiconductor device as claimed in claim 1 wherein said encapsulant occupies substantially all of said void.

6. A packaged semiconductor device as claimed in claim 1 wherein said semiconductor chip is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

7. (Amended) A packaged semiconductor device comprising:
a semiconductor chip;

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a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer and said underlying substrate, and

at least one void formed in said laminate so as to extend from said first major face through said solder resist layer, through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

8. A packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

9. A packaged semiconductor device as claimed in claim 8 wherein said at least one void extends from said first major face through said laminate to said second major face and wherein said encapsulant is positioned to extend through said void from said first major face to said second major face.

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10. A packaged semiconductor device as claimed in claim 8 wherein said contact between said encapsulant and said laminate is characterized by an adhesive bond.

11. A packaged semiconductor device as claimed in claim 8 wherein said encapsulant occupies substantially all of said void.

12. A packaged semiconductor device as claimed in claim 8 wherein said semiconductor chip is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

13. (Amended) A packaged semiconductor device comprising:

a semiconductor chip;

an FR-4 epoxy-glass laminate defining first and second major faces and including a plurality of laminated epoxy layers, said epoxy laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated epoxy layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said epoxy resin glass-cloth laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated epoxy layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

23. (Amended) A computer including at least one packaged semiconductor device comprising:

a semiconductor chip;

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer,

at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate, and through said second major face; and

an encapsulant positioned to mechanically couple said semiconductor die to said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

Remarks

Information Disclosure Statement

The Office Action stated the information disclosure statement filed on 9/20/99 failed to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609. The Applicant has spoken with the Examiner regarding this matter and has faxed in copies of the PTO 1449 form and the return receipt card date stamped September 20, 1999 by the PTO, thereby proving its timely submission to the Examiner.

Title of the Invention

The Office Action objected to the title of the invention. The Applicant has amended the title of the invention as suggested by the Examiner.

Claim Rejections - 35 USC § 102

Claims 1-13 and 23 were rejected under 35 U.S.C. 102(b) as being anticipated by Juskey et al., U.S. Patent No. 5,336,931, hereinafter referred to as Juskey.

The Applicant has amended claim 1 to form a void "from a first major face through said underlying substrate and through said second major face." This claim language is shown in Fig. 2. Juskey fails to disclose and suggest, explicitly or implicitly,

such a claim limitation. Juskey only shows forming an anchor hole 150 in a substrate 160, and teaches that the lower solder mask 190 covers the anchor hole 150 and thereby acts as a bottom to the anchor 150 to prevent the cover forming material from flowing out through the bottom of the anchor hole 150 during the flow forming of the cover 110. See column 4, lines 2-9. In view of the cited prior the Applicant submits that claim 1 as amended is allowable and thus requests that the anticipation rejection to this claim, and the remaining claims that depend therefrom, namely claims 4-6, be removed. Please note, claims 2 and 3 have been canceled.

With regards to claim 7, the Applicant has amended this claim to include forming a void "so as to extend from said first major face one through said solder resist layer, through said electrically conductive layer, through said underlying substrate and through said second major face." As mentioned above, Juskey fails to disclose such a claim limitation by teaching forming only an anchor hole 150 in a substrate 160. As such, the Applicant requests that this rejection of claim 7 also be removed.

Claim 8 recites "a laminate ... including a plurality of laminated layers." The plurality of laminated layers is shown in Fig. 2 and described on page 9, lines 13-24 of Applicant's specification. Juskey fails to disclose, teach, and/or suggest, explicitly or implicitly, a laminate including a plurality of laminated layers. Furthermore, the Applicant notes that the Office Action even fails to allege that Juskey teaches a plurality of laminated layers. Additionally, the Applicant notes that Juskey only discloses that the substrate may be manufactured using a material such as a Bismaleimid Triazine Epoxy laminate. Thus, the Applicant requests that this rejection of claim 8 be removed. Claims 9-12 depend from claim 8 and are allowable for the same reasons.

The Applicant has amended claim 13 to recite "an FR-4 epoxy -glass laminate." Juskey fails to disclose an FR-4 epoxy -glass laminate. Juskey only discloses a Bismaleimid Triazine Epoxy laminate. As such, the Applicant respectfully requests that this rejection be removed.

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The Applicant has amended claim 23 to recite "a void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate, and through said second major face." As mentioned above, Juskey fails to disclose such a claim limitation by teaching only forming an anchor hole 150 in a substrate 160. Therefore, the Applicant also requests the rejection of claim 23 be removed.

Conclusion

The Applicant respectfully submits that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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By _____

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